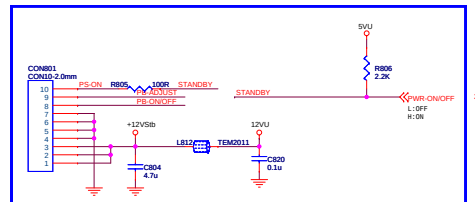
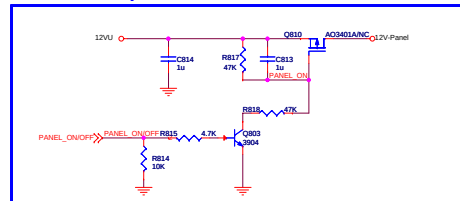


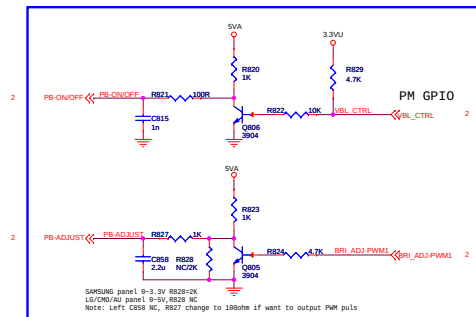
Connettor



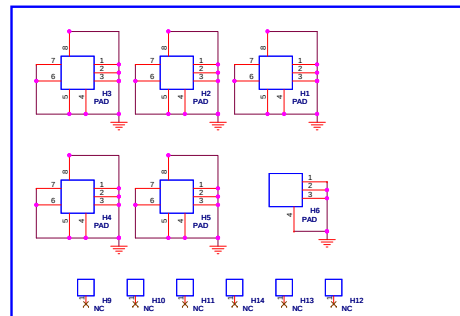
Power for panel



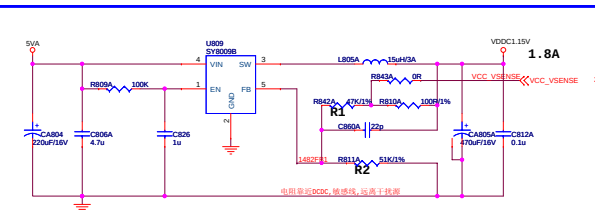
Inverter controller



Hole & Mark



DC/DC



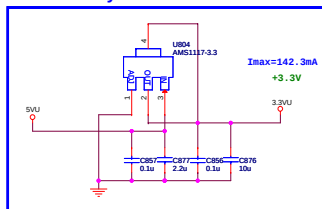
SY8009: $V_{out}=0.6V \cdot (1+R1/R2)$

R810=100, R842=47k, R811=51K, Vout=1.154V

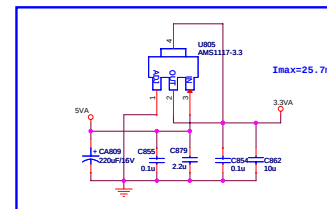
To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R1 and R2. A value of between 10k and 1M is highly recommended for both resistors.

LDO

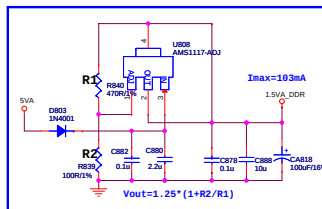
3.3V Standby Power



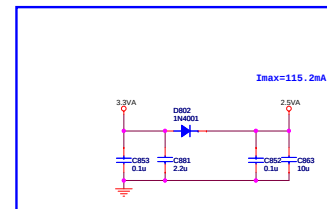
3.3V Normal Power



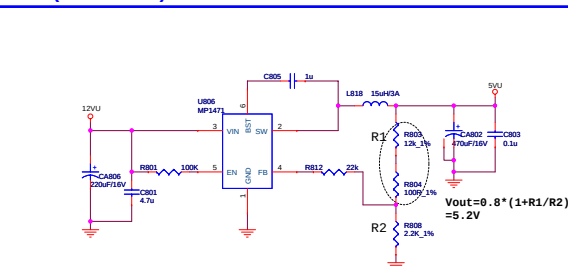
1.5V Normal Power for DDR3



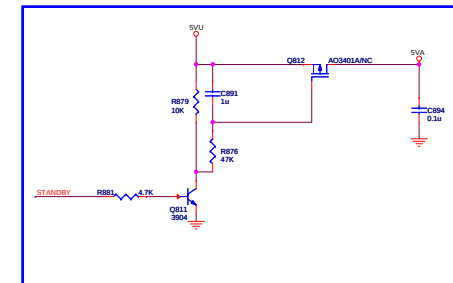
2.5V Normal Power for ADC



DC/DC (12V - - 5V)



POWER SWITCH



The diagram illustrates the pin connections for a USB to CVBS module. The central module has the following pins and connections:

- VGA:**
 - VGA_R1 (Red) to R1
 - VGA_R2 (Red) to R2
 - VGA_G1 (Green) to G1
 - VGA_G2 (Green) to G2
 - VGA_B1 (Blue) to B1
 - VGA_B2 (Blue) to B2
- USB:**
 - USB_DP+ (Data+) to D+
 - USB_DP- (Data-) to D-
 - USB_DM+ (Data+) to D+
 - USB_DM- (Data-) to D-
 - USB_VCC (Power) to VCC
 - USB_GND (Ground) to GND
- YPbPr:**
 - YPbPr_Y (Yellow) to Y
 - YPbPr_Pb (Blue) to Pb
 - YPbPr_Pr (Red) to Pr
- CVBS:**
 - CVBS_Y (Yellow) to Y
 - CVBS_Pb (Blue) to Pb
 - CVBS_Pr (Red) to Pr
- SCART:**
 - SCART_Y (Yellow) to Y
 - SCART_Pb (Blue) to Pb
 - SCART_Pr (Red) to Pr
- Audio:**
 - Audio_L (Left) to L
 - Audio_R (Right) to R

A green box highlights the CVBS connections, showing the following wiring:

- CVBS_Y (Yellow) to Y
- CVBS_Pb (Blue) to Pb
- CVBS_Pr (Red) to Pr

The diagram illustrates the CRISPR-Cas9 system. The top part shows the CRISPR array with a repeat (red) and spacer (blue) region, flanked by Cas9 (red) and Cas2 (blue) genes. The bottom part shows the CRISPR array after deletion of a repeat, labeled "Deleting Part 1" and "Deleting Part 2".

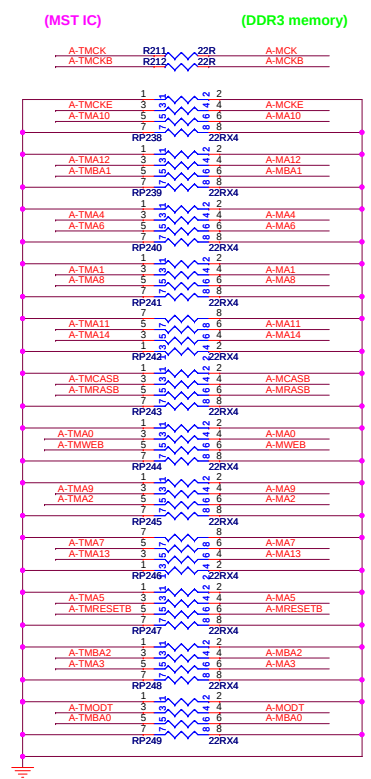
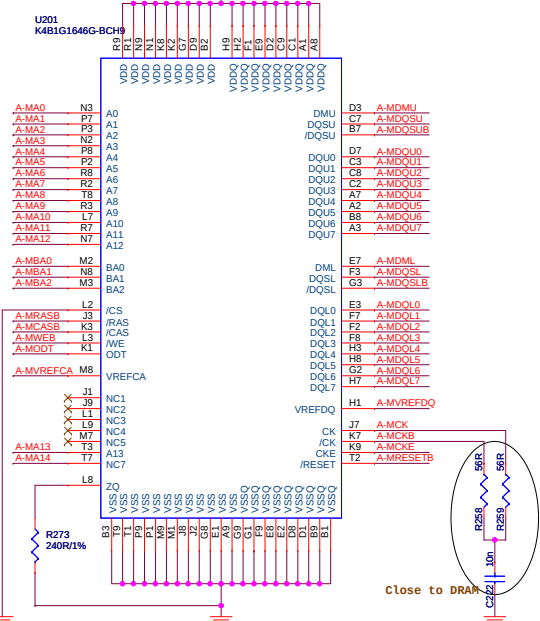
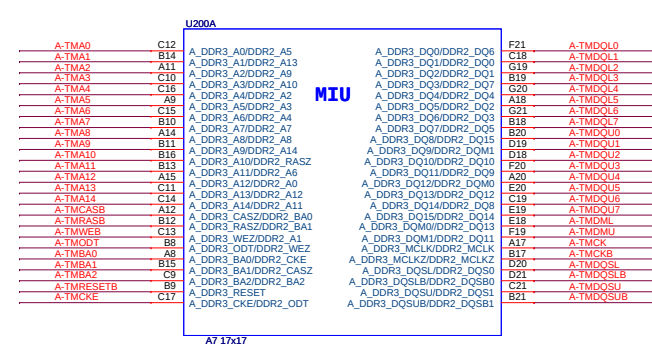
[illegible][illegible]

```
// CS2P Config (125.00K MCK, 125.00K MCK, PAD_PWD1, PAD_PWD0)
SPL1_M0_0.2 0*00000 Boot from BG05 with SPI Flash
SPL1_M0S 0*00001 Secure BG1 without scramble
SPL1_M0 0*00000 Secure BG1 with scramble

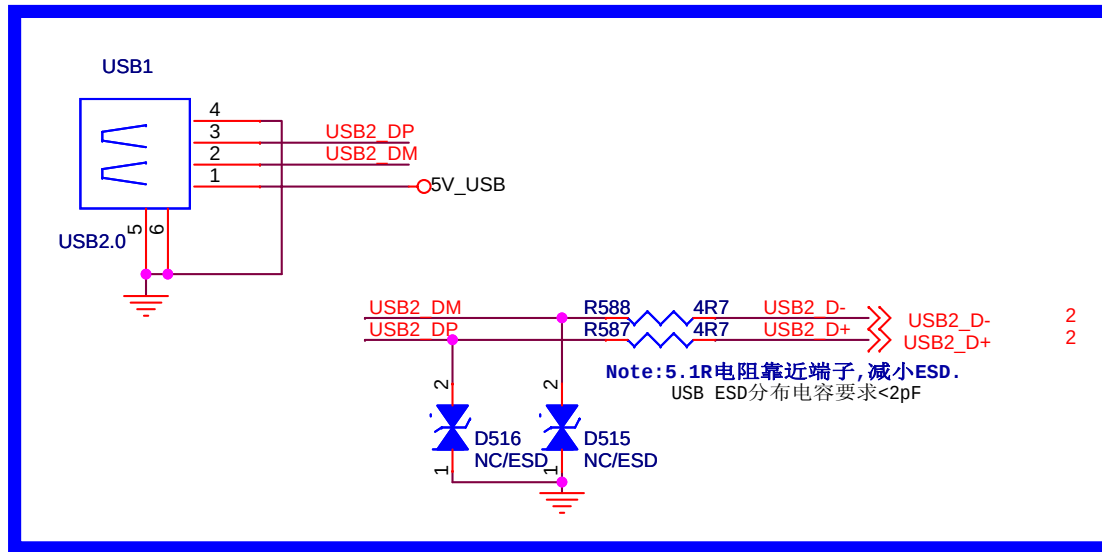
NPS1_SPL1_M0_0.2 0*00000 Boot from NPS1 with SPI Flash
NPS1_SPL1_M0S 0*00001 Boot from NPS1 with SPI Flash
NPS1_SPL1_M0 0*00000 Secure BG1 with SPI Flash

NPS1_M0S 0*00001 Secure NPS1 without scramble
NPS1_M0 0*00000 Secure NPS1 with scramble
NPS1_WD 0*00001
```

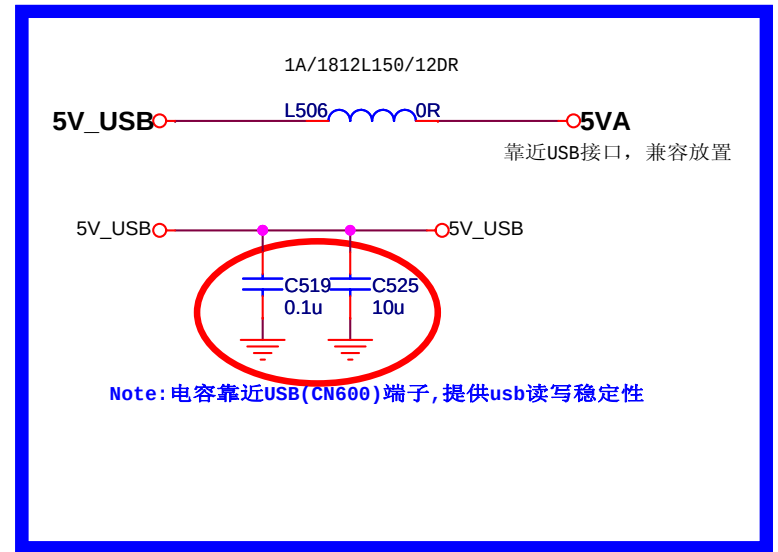
The diagram illustrates a 16-bit parallel adder implemented using a 74181 ALU. The ALU is a 4-bit device with two 4-bit data inputs (A and B), a 4-bit data output (Y), a 4-bit carry-in (Cin), and a 4-bit carry-out (Cout). The carry-in is connected to a 16-bit bus labeled 'CARRY IN'. The carry-out is connected to a 16-bit bus labeled 'CARRY OUT'. The ALU is also connected to a 16-bit bus labeled 'DATA'. The ALU is shown with its internal structure, including a 16-bit data path and a 4-bit carry path. The ALU is labeled '74181 ALU'.



USB Interface



USB POWER



深圳市高新区南区科技南十路国际技术创新研究院C座4楼

TEL:0755-26996895 FAX:0755-26996830

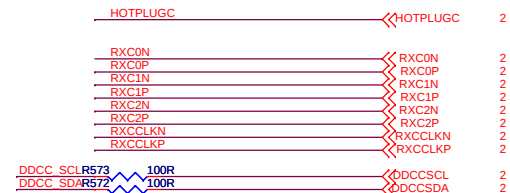
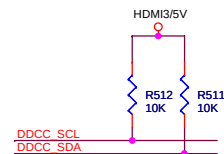
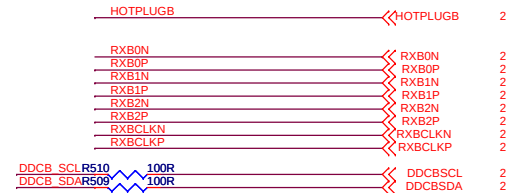
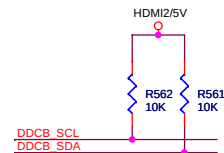
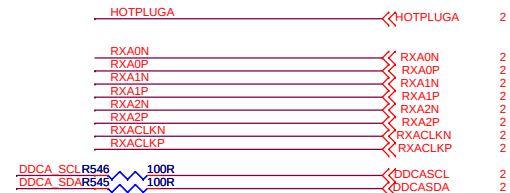
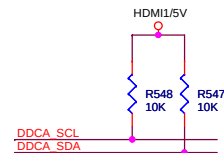
Title MSD306BTM

Size Document Number

Rev
1.0

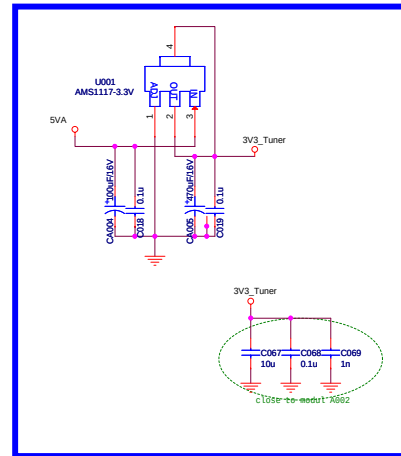
Date: Friday, April 12, 2013

Sheet 5 of 17

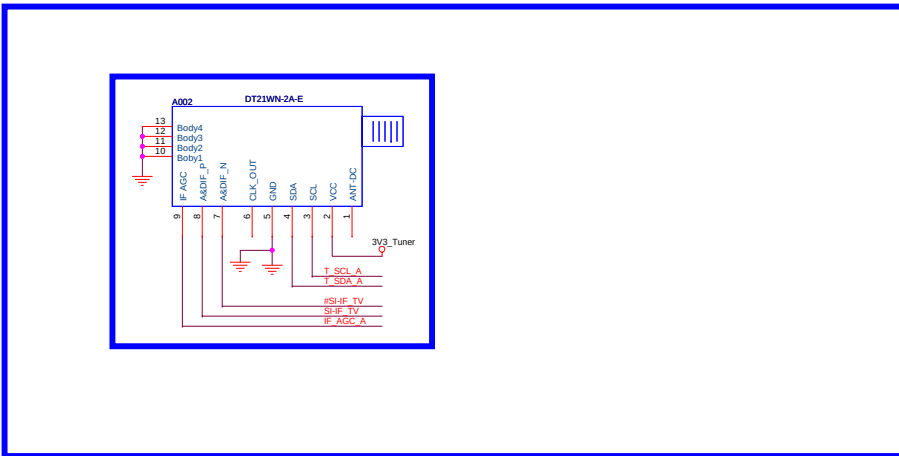


HDMI-ARC C599 NC/1u R599 NC/0R HDMI-ARC HDMI-ARC 2011-11-15

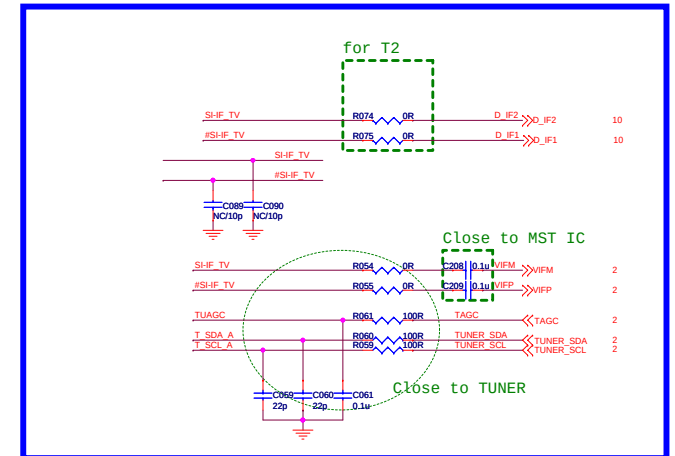
Tuner Power



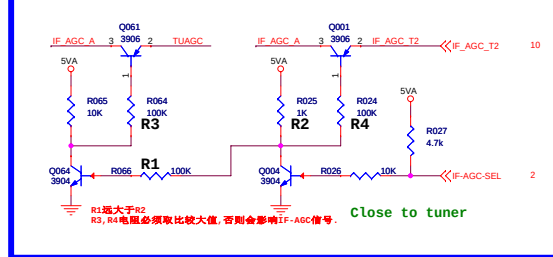
Silicon in can Tuner



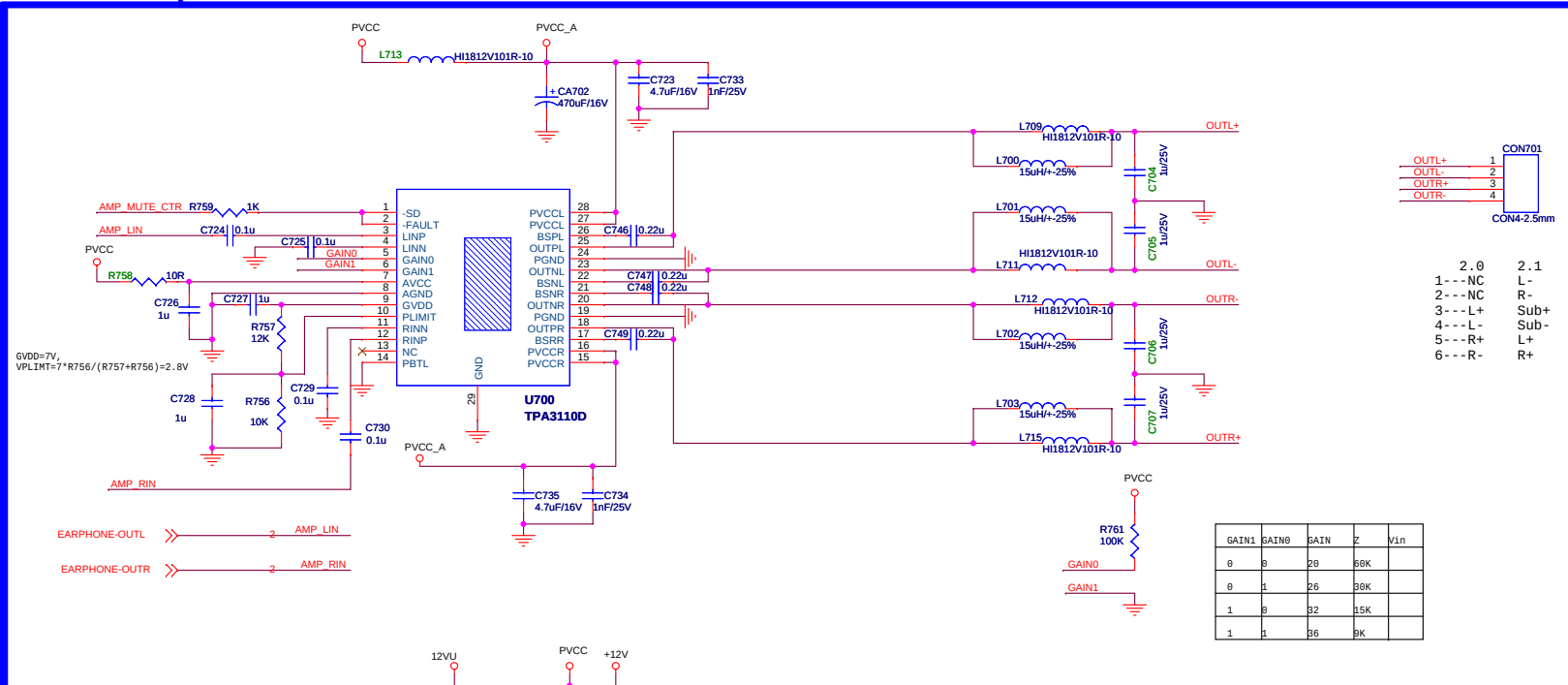
IF AGC Switch



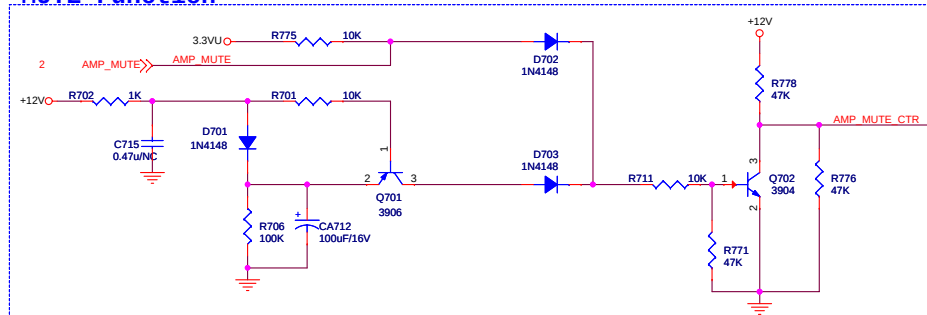
IF AGC Switch



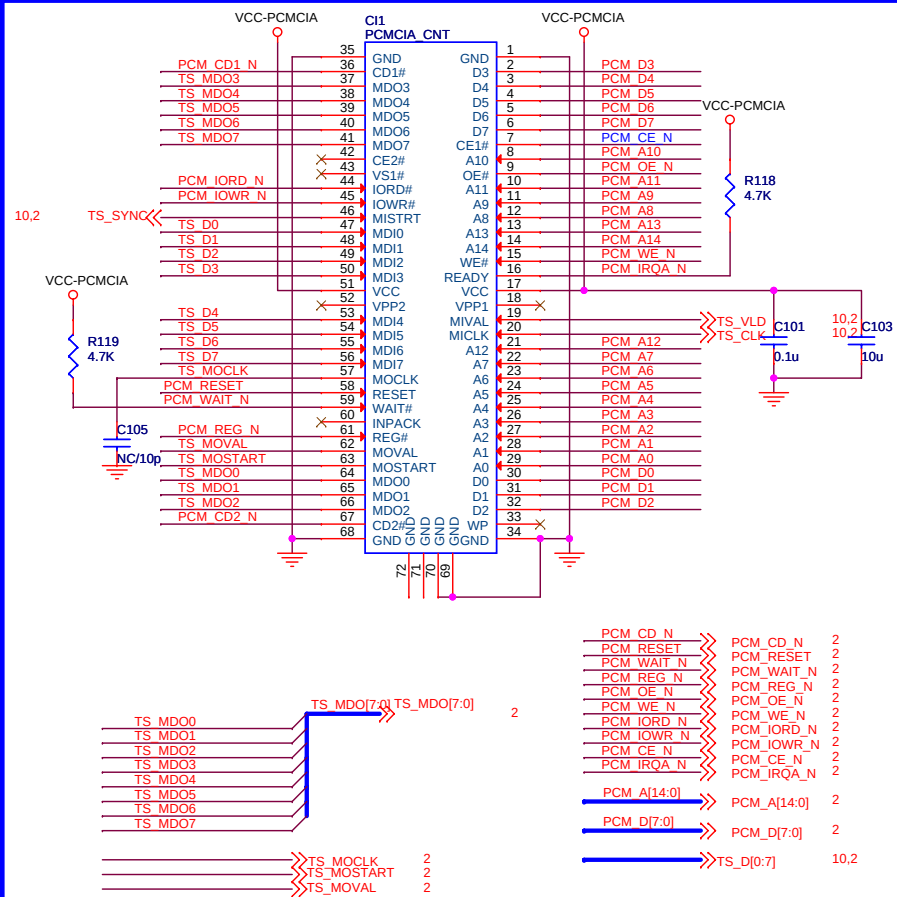
Power Amplifier



MUTE Function



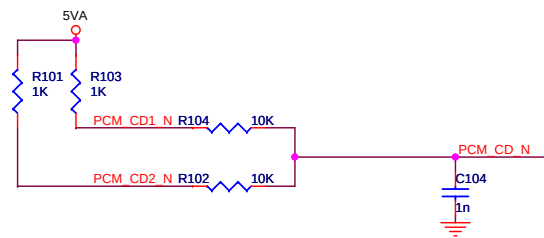
PCMCIA



PCMCIA POWER

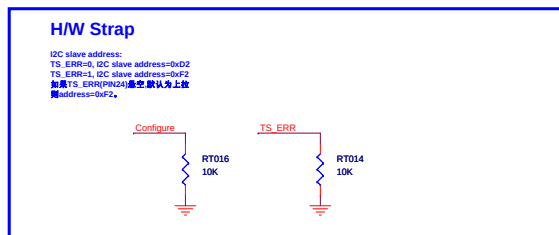
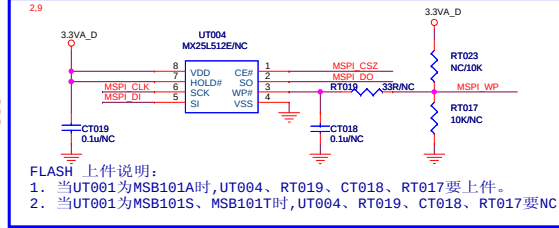
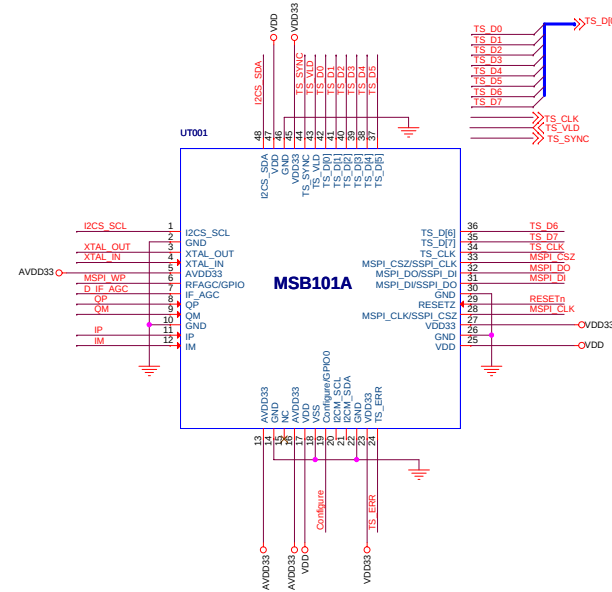
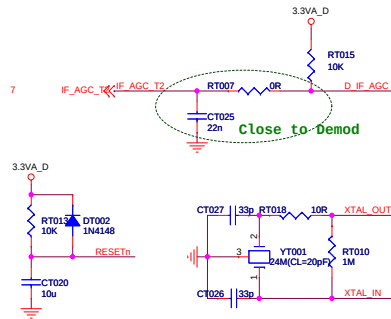
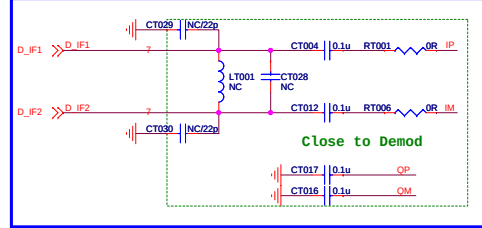


CARD DETECT



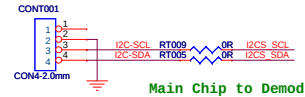
PCM_CD1_N	PCM_CD2_N	PCM_CD_N
GND	GND	L 0V
GND	NC	H 2.5V
NC	GND	H 2.5V
NC	NC	H 5V

DVB-T/T2/C



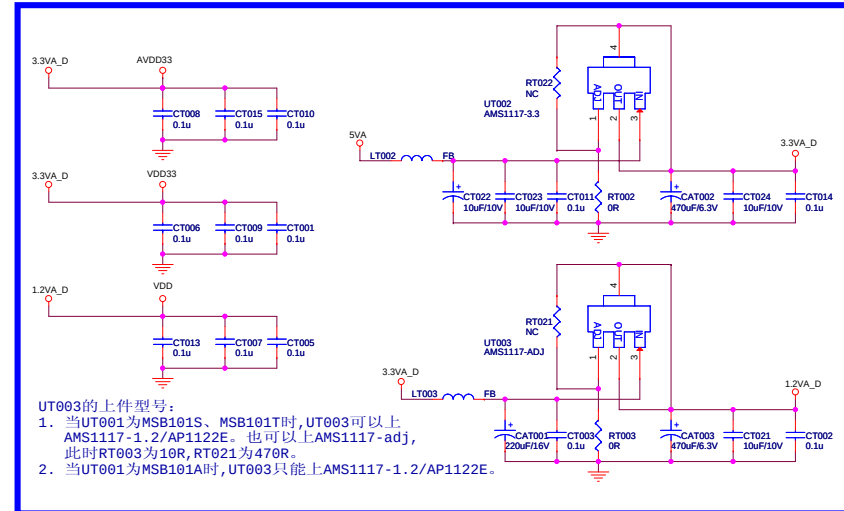
I2C-SDA I2C-SDA 2
I2C-SCL I2C-SCL 2

Debug port



Demod to Tuner

POWER



UT003的上件型号:

1. 当UT001为MSB101S、MSB101T时,UT003可以上AMS1117-1.2/AP1122E。也可以上AMS1117-adj,此时RT003为10R,RT021为470R。
2. 当UT001为MSB101A时,UT003只能上AMS1117-1.2/AP1122E。

Edition Ifomation	
VER3	1, R054, R055封装更改为0402封装。 2, C217的封装更改为0603封装。 3, 增加贴片电容C884、C885、C886、C887、C888。 4, 删除贴片电容C088。 5, 删除插座CON201。
VER3	(only silicon in can)2012-2-21
	1,删除silicon on bord 部分电路（TDA18273及外围电路） 2, 兼容TCL及长虹Silicon in can modul 3, 为了通过S2A测试，增加贴片电容C329、C330 4, 增加贴片电阻R707 5, 增加贴片电阻R715、R717,贴片二极管D706、D707 6, 增加铝电解电容CA704
VER4	1,在VER3的基础上兼容3D屏,标准化LVDS插座！ 2, 删除了插座CON204

Title		
A7 17x17		
Size A	Document Number <Doc>	Rev <RevCode>
Date:	Friday, April 12, 2013	Sheet 17 of 17